Abstract

We describe a programmable multi-chip VLSI neuronal system that can be used for exploring spike-based information processing models. The system consists of a silicon retina, a PIC microcontroller, and a transceiver chip whose integrate-and-fire neurons are connected in a soft winner-take-all architecture. The circuit on this multi-neuron chip approximates a cortical microcircuit. The neurons can be configured for different computational properties by the virtual connections of a selected set of pixels on the silicon retina. The virtual wiring between the different chips is effected by an event-driven communication protocol that uses asynchronous digital pulses, similar to spikes in a neuronal system. We used the multi-chip spike-based system to synthesize orientation-tuned neurons using both a feedforward model and a feedback model. The performance of our analog hardware spiking model matched the experimental observations and digital simulations of continuous-valued neurons. The multi-chip VLSI system has advantages over computer neuronal models in that it is real-time, and the computational time does not scale with the size of the neuronal network.

1 Introduction

The sheer number of cortical neurons and the vast connectivity within the cortex are difficult to duplicate in either hardware or software. Simulations of a network consisting of thousands of neurons with a connectivity that is representative of cortical neurons can take minutes to hours on a fast Pentium, particularly if spiking behavior is simulated. The simulation time of the network increases as the size of the network increases. We have taken initial steps in mitigating the simulation time of neuronal networks by developing a multi-chip VLSI system that can support spike-based cortical processing models. The connectivity between neurons on different chips and between neurons on the same chip are reconfigurable. The receptive fields are effected by appropriate mapping of the spikes from source neurons to target neurons. A significant advantage of these hardware simulation systems is their real-time property; the simulation time of these systems does not increase with the size of the network.

In this work, we show how we synthesized orientation-tuned spiking neurons using the multi-chip system in Figure 1.